DERWENT-ACC-NO: 1989-302301

DERWENT-WEEK: 200001

TITLE: Integrated CMOS bridge circuit e.g. for driving small electric motor - has second region having same doping and depth as first region and being electrically connected to source of second FET

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The integrated CMOS circuit comprises a transistor (T2) located in a p (or an n) well (5) and an adjacent complementary transistor (T1). The transistors are located in an epitaxial layer (4) on a highly doped substrate (2). The bridge circuits having an inductive load, parasitic currents can occur, which give rise to 'latch-up' and/or dissipation.

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The semiconductor device comprises at least one pair of complementary insulated gate field effect transistors. The device has a semiconductor body with a highly doped substrate of a first conductivity type, a less highly doped epitaxial layer of the first conductivity type on it and adjoining a surface of the body and a first region of a second, opposite conductivity type, which also

adjoins the surface and is entirely surrounded within the semiconductor body by
the epitaxial layer. Source and drain zones of the first conductivity type of
a first insulated gate field effect transistor of the pair are provided within
the first region and source and drain zones of the second conductivity type of
a second insulated gate field effect transistor of the pair are provided beside
the first region.

DOCUMENT-IDENTIFIER: US 20020137349 A1

TITLE: Monolithic low dielectric constant platform for passive components and method

---------- KWIC ---------

[0014] Silicon substrates are typically provided with a lightly doped epitaxial layer for formation of active components (e.g., transistors and the like). A more heavily doped substrate is usually employed to support the epitaxial layer and to provide a low resistance ground return path for components formed in the epitaxial layer. Additionally, a highly doped substrate aids in prevention of latch-up phenomena.

US-PAT-NO: 3920481

DOCUMENT-IDENTIFIER: US 3920481 A

TITLE: Process for fabricating insulated gate field effect transistor
structure

---------- KWIC ---------

Conventional complementary field effect devices are fabricated as
conductor-insulator-semiconductor structures with interconnections between
particular sources or drains of the n-channel and p-channel devices. The
conductors may be metal or conductive polycrystalline silicon. Silicon dioxide
is the most widely used insulator, and single crystal silicon is the most
widely used semiconductor substrate. Typical complementary metal oxide
semiconductor (CMOS) structures are fabricated on an n-type substrate rather
than on a p-type substrate because it is easier to obtain desirable threshold
voltages for both the n-channel and p-channel complementary devices. The
p-well required for the n-channel complement is obtained by diffusing a lightly
doped p-region into the n-type substrate. In some devices all n-channel
devices are fabricated in a common p-well, and p-channel devices are fabricated
in the n-substrate so that much of the overall area is taken up with
interconnections between the n-channel and p-channel devices. Where individual
p-wells are used for the n-channel devices, isolation of the p-channel
field-effect transistors is sometimes achieved by heavily doped channel stops.
These channel stops occupy a large amount of wafer surface area, degrade

operating speed and limit the voltage range. Recently, polycrystalline silicon
has been used in place of metal for the gate electrode of the devices, but
although transient performance is slightly improved, a negligible reduction in
area has been effected. Also, the standard dopant, boron, which is placed in
the polycrystalline silicon to render it conductive and to obtain a low
threshold, possesses the property that it may diffuse through the gate oxide in
the presence of hydrogen and degrade the device. And, prior-art CMOS devices
are known to experience impurity migration through both the gate and field
oxides with resultant impairment of the operating characteristics of the
devices. Finally, the presence of uncontrolled amounts of fixed surface state
charges, due typically to non-stoichiometric composition of the SiO.sub.2, also
impairs the operating characteristics of the devices.

US-PAT-NO: 4266237

DOCUMENT-IDENTIFIER: US 4266237 A

TITLE: Semiconductor apparatus

---------- KWIC ----------

FIG. 1 shows a semiconductor material substrate, 10, which is usually silicon
doped with boron to have a p-type conductivity. Typically, the resistivity of
substrate 10 will be between 4 and 12 ohm-cm. The silicon is typically
Czchrolski grown and has a major surface, 11, which is a (100) plane through
and on which any fabrication process, resulting in circuit components
associated with the substrate, will take place.

US-PAT-NO: 4435895

DOCUMENT-IDENTIFIER: US 4435895 A

TITLE: Process for forming complementary integrated circuit devices

---------- KWIC ---------

To this end, the silicon bulk region 11, which is n-type and of relatively low
resistivity, first has grown thereon a lightly doped epitaxial n-type layer 12.
The use of relatively lightly doped epitaxial layer on a relatively heavily
doped substrate of the same resistivity type is known to provide protection
against parasitic SCR-type latchup in CMOS devices.

US-PAT-NO: 5061646

DOCUMENT-IDENTIFIER: US 5061646 A

TITLE: Method for forming a self-aligned bipolar transistor

---------- KWIC ---------

Various aspects of the invention will now be described in detail with reference to the FIGURES. An understanding of the invention can be obtained through the explanation of the fabrication of a single vertical bipolar device as illustrated in FIGS. 1-8; however, it will be understood that an integrated circuit contains many such devices and that both PNP and NPN devices may be present depending on the circuit being implemented. Moreover, BiCMOS integrated circuits contain PMOS and NMOS transistors whose construction is fully compatible with the described fabrication sequence. Further, the devices can be fabricated on a conventional substrate commonly used in semiconductor manufacturing sciences such as a single crystal substrate, either N or P-type, having an overlying epitaxial layer. Additionally, the substrate can have a buried insulating layer between the semiconductor body and the overlying epitaxial layer, or alternatively, the substrate can comprise an insulating body such as sapphire supporting the epitaxial layer.

US-PAT-NO: 5223737

DOCUMENT-IDENTIFIER: US 5223737 A

TITLE: Electrostatic discharge protection device for an integrated circuit pad
and related integrated structure

---------- KWIC ---------

A preferred implementation of the invention is shown in FIGS. 7A, 7B and 7C, in
which is represented a typical application of the protection device of the
invention to a pad of a circuit, integrated in an n.sup.- type epitaxial layer
formed on a monocrystal semiconductor substrate (commonly having a p.sup.- type
conductivity). This in fact represents the type of semiconductor substrate
most widely used to fabricate integrated circuits and in particular to
fabricate so-called BCD type integrated circuits (containing bipolar, CMOS and
DMOS structures integrated on the same monolithic substrate). Naturally, as
will clearly be apparent to the expert, the protection device of the invention
can be embodied in a circuit, integrated into a p type conductivity epitaxial
layer, by inverting all conductivities and polarities of the respective circuit
nodes (and the direction of the currents).

US-PAT-NO: 5702982

DOCUMENT-IDENTIFIER: US 5702982 A

TITLE: Method for making metal contacts and interconnections concurrently on semiconductor integrated circuits

---------- KWIC ---------

Starting with FIG. 1, a schematic cross-sectional view is shown of a portion of a semiconductor substrate 10 having partially completed device contact areas and field oxide isolation regions. The most widely used substrate in the semiconductor industry is composed of single crystal silicon having, for example, a <100> crystallographic axial orientation. The silicon is usually conductively doped with N-type dopants, such as arsenic, or P-type dopants, such as boron. Integrated circuits, such as dynamic random access memory (DRAM), static random access memory (SRAM), microprocessors and the like are then built in and on the silicon substrate. However, it should be well understood by those skilled in the art that the method of this invention is equally applicable to other types of substrates where multilevel wiring is required. For the purpose of this invention a silicon substrate is used.

US-PAT-NO: 6121073

DOCUMENT-IDENTIFIER: US 6121073 A

TITLE: Method for making a fuse structure for improved repaired yields on
semiconductor memory devices

---------- KWIC ---------

Shown in FIG. 2 is a portion of a semiconductor substrate 10 having a partially
completed fuse structure. These fuse structures are formed over a Field OXide
(FOX) isolation region 12 used to electrically isolate the device areas on the
substrate. The most widely used substrate in the semiconductor industry is
composed of single-crystal silicon having, for example, a <100>crystallographic orientation. Typically the substrate 10 is doped
P.sup.- for making integrated circuits such as random access memory (RAM)
devices, but the method for making these improved fuse structures is equally
applicable on other types of substrates. The FOX 12 surrounding the device
areas can be formed by various means. For example, one method is the LOCal
Oxidation of Silicon (LOCOS) technique in which a stress-release pad oxide and
a silicon nitride (Si.sub.3 N.sub.4) layer (not shown) are patterned to form an
oxidation barrier mask over the device areas. The exposed regions of the
silicon substrate 10 are then oxidized, for example by steam (wet) oxidation,
to form the field oxide 12, as shown in FIG. 2 after removal of the silicon
nitride layer. Typically the FOX isolation is grown to a thickness of between
about 4000 and 5000 Angstroms. Alternative methods of forming the FOX
isolation can be employed, such as shallow trench isolation

(STI) commonly used
in the industry. However, for the purpose of this
invention, the LOCOS method
is used to form the FOX isolation 12.

US-PAT-NO: 6159385

DOCUMENT-IDENTIFIER: US 6159385 A

TITLE: Process for manufacture of micro electromechanical devices having high electrical isolation

---------- KWIC ---------

Carrier substrate 106 is either a p-type or n-type silicon wafer such as is commonly used in semiconductor processing; the orientation and conductivity of the wafer will, of course, depend on the specific application. Using known semiconductor processing techniques, a silicon layer 108 is grown on carrier substrate 106. Layer 108 may be doped with boron, germanium or other known dopants to impart an etch stop and semiconductor properties. Using semiconductor device manufacturing techniques, electrical components such as resistors, capacitors, inductors or interconnects may be readily formed. An optional silicon dioxide layer 110 is grown on top of silicon layer 108 and an organic adhesive layer 112 is spun on top. The silicon dioxide layer may be eliminated if the rigidity of the MEM component is not critical. Further, either adhesive layer 104 or 112 may omitted from the process since only one layer may be necessary in some applications.

US-PAT-NO: 6169318

DOCUMENT-IDENTIFIER: US 6169318 B1

TITLE: CMOS imager with improved sensitivity

---------- KWIC ---------

A simple CMOS technology employs two basic types of FET's, namely n-MOS FET's and p-MOS FET's. Most CMOS processes start with a p-doped substrate or with a p-type epitaxial layer deposited by known methods on a substrate of a different doping-type, such as an insulating or n-type substrate, with the substrates predominantly made of silicon. The p-dopant level of the substrate is typically around 1.times.10.sup.15 cm.sup.-3. Other substrates, for example sapphire, can also serve as carriers for the p-type epitaxial layer. Both the p-doped substrate and the p-type epitaxial layer with hereinafter be referred to as p-substrate. N-MOS FET's are built in the uniformly doped p-type substrate through patterning of an active window with a gate oxide having an active gate disposed thereon, wherein the active area not covered by the gate is subsequently doped n.sup.+ -type by known methods to a level of typically 1.times.10.sup.19 to 1.times.10.sup.21 cm.sup.-3. P-MOS FET's are built in an n-type well formed in the p-doped substrate through patterning of an active window with a gate oxide having an active gate disposed thereon, wherein the active area not covered by the gate is subsequently doped p-type.

US-PAT-NO: 6406954

DOCUMENT-IDENTIFIER: US 6406954 B1

TITLE: Method for forming out-diffusing a dopant from the doped polysilicon
into the N-type and P-type doped portion

---------- KWIC ---------

Modern semiconductive processing methods frequently involve formation of n-type
diffusion regions and p-type diffusion regions in a semiconductive material, as
well as formation of transistors associated with the n-type diffusion regions
and p-type diffusion regions. Monocrystalline silicon wafers are commonly
utilized as semiconductive substrates, with the wafers generally being lightly
background doped with p-type conductivity-enhancing dopant. At various regions
within a wafer, an n-type conductivity-enhancing dopant can be implanted to a
concentration which overwhelms the p-type dopant to thereby form n-wells. In
other regions of the wafer the n-type dopant is not implanted, and such other
regions remain as p-type regions (which can be referred to as p-wells).

EP 271749

DERWENT-ACC-NO: 1988-169055

DERWENT-WEEK: 198825

TITLE: Improving integrated electronic device performance - by segregation of metallic impurities from junction regions

---------- KWIC ----------

A integrated electronic device, i.e. CMOS device, has a heavily doped layer of P/P epitaxial substrate doped with B or of N/N epitaxiated substrate doped with P. The gettering abilities in the region of the heavily doped substrate during the low temp. processing steps and the final annealing steps are utilised for the segregation and ultimate removal of the undesired metallic impurities in the heavily doped region.